Problems

1. Consider an n-type MOSFET, which consists of a 10 nm thick oxide ($\varepsilon_r = 3.9$) and has a gate length of 1 micron, a gate width of 20 micron and a threshold voltage of 1.5 Volt. Calculate the resistance of the MOSFET in the linear region as measured between source and drain when applying a gate-source voltage of 3 Volt. What should the gate-source voltage be to double the resistance? The surface mobility of the electrons is 300 cm^2/V-sec.

2. Consider an n-type MOSFET with an oxide thickness $t_{ox} = 20$ nm ($\varepsilon_r = 3.9$) and a gate length, $L = 1$ micron, a gate width, $W = 10$ micron and a threshold voltage, $V_T = 1$ Volt. Calculate the capacitance per unit area of the oxide, C_{OX}, and from it the capacitance of the gate, C_G. Calculate the drain current, I_D, at a gate-source voltage, $V_{GS} = 3$ Volt and a drain-source voltage, $V_{DS} = 0.05$ Volt. The surface mobility of the electrons $\mu_n = 300$ cm^2/V-sec. Use the linear model of the MOSFET.

3. A MOSFET ($L = 1$ μm, $t_{ox} = 15$ nm, $V_T = 1$ V and $\mu_n = 300$ cm^2/V-sec) must provide a current of 20 mA at a drain-source voltage of 0.5 Volt and a gate-source voltage of 5 Volt. How wide should the gate be?

4. A MOSFET ($L = 1$ μm, $t_{ox} = 10$ nm, $V_T = 1$ V and $\mu_n = 300$ cm^2/V-sec) is to be used as 50 Ω terminating resistor when applying a gate-source voltage, $V_{GS} = 5$ Volt. How wide should the gate be?

5. The capacitance of an n-type silicon MOSFET is 1 pF. Provided that the oxide thickness is 50 nm and the gatelength is 1 micron, what is the resistance of the MOSFET in the linear regime when biased at a gate voltage which is 5 Volt larger than the threshold voltage? Use an electron surface mobility of 500 cm^2/V-sec.

6. Consider a p-channel silicon MOSFET with an aluminum gate.

   a) Draw the energy band diagram of the MOS structure for $V_G = V_{FB}$. Indicate the workfunction of the metal and the semiconductor, as well as the electron affinity.

   b) Draw the field distribution for $V_G = V_T$ (onset of inversion).

   c) Calculate the depletion layer width and the field in the oxide at the onset of inversion. ($N_d = 10^{16}$ cm^{-3}, $t_{ox} = 100$ nm, $V_{FB} = -0.5$V)

7. Calculate the depletion region width within a p-type bulk silicon MOS- capacitor with $N_d = 10^{17}$ cm^{-3}, at the onset of inversion.

8. A silicon p-substrate ($p \cong N_a = 10^{16}$ cm^{-3}) MOSFET with $t_{ox} = 0.1$ μm, $\varepsilon_{ox}/\varepsilon_0 = 3.9$ and a negative interface charge per unit area of -10^{-8} C/cm^2, has a threshold voltage which is 1 Volt smaller than desired. By what value should one change the oxide thickness to obtain the desired threshold voltage? Should one increase or decrease the oxide thickness?

9. A silicon MOSFET ($n_i = 10^{10}$ cm^{-3}, $\varepsilon_s/\varepsilon_0 = 11.9$ and $\varepsilon_{ox}/\varepsilon_0 = 3.9$) is scaled by reducing all dimensions by a factor of 2 and by increasing the doping density of the substrate by a factor of 4.

   Calculate the ratio of the following parameters of the scaled device relative to that of the original device: (make approximations if necessary)

a) The transconductance at $V_{GS} - V_T = 1$ V.

b) The gate capacitance

c) The transit frequency at $V_{GS} - V_T = 1$ V. (Assume that $C_{DS} = 0$)

d) The threshold shift when increasing the reverse bias of the source-bulk diode from 1 Volt to 3 Volt.

e) The breakdown voltage of the oxide assuming the breakdown field to be constant.

f) The breakdown voltage of the drain-to-bulk p-n diode assuming the breakdown field to be constant.

10. A silicon p-substrate ($p \cong N_a = 10^{16}$ cm^{-3}) MOSFET with $t_{ox} = 0.1$ µm, $\varepsilon_{ox}/\varepsilon_0 = 3.9$ and $V_{FB} = -0.2$ V, has a threshold voltage which is 1 Volt smaller than desired. By what value should one change the oxide thickness, t_{ox}, to obtain the desired threshold voltage? Should one increase or decrease the oxide thickness?

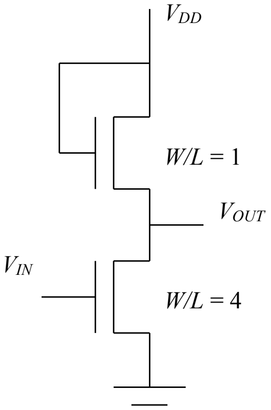
11. Two n-type MOSFETs are connected as shown below in a configuration known as an enhancement-load inverter.

a) Calculate the relation between the output voltage and the input voltage assuming that both transistors are in saturation

b) Find the maximum input voltage, V_{in}, and the corresponding output voltage, V_{out}, for which both transistors are in saturation.

Use $K = 10$ mS, $V_T = 1$ V, $V_{DD} = 10$ V.

The width-to-length ratios of the transistors are indicated on the figure.



12. Consider a p-channel silicon MOSFET with an aluminum gate ($\Phi_M = 4.1$ V, $\chi = 4.05$ V,

$\varepsilon_{ox}/\varepsilon_0 = 3.9$, $\varepsilon_s/\varepsilon_0 = 11.9$, $n_i = 10^{10}$ cm^{-3}, $N_d = 10^{17}$ cm^{-3}, $t_{ox} = 100$ nm, $V_{FB} = -0.5$V).

a) Draw the electric field distribution for $V_G = V_T$ (onset of inversion).
b) Calculate the electric field in the oxide at the onset of inversion.

13. Consider an n-type MOSFET, which consists of a 10 nm thick oxide and has a gate length of 1 micron, a gate width of 50 micron and a threshold voltage of 1 Volt. Calculate the resistance of the MOSFET in the linear region as measured between source and drain when applying a gate-source voltage of 3 Volt. ($\mu_n = 300$ cm^2/V-s, $\varepsilon_{ox}/\varepsilon_0 = 3.9$)

14. A silicon MOSFET ($n_i = 10^{10}$ cm^{-3}, $\varepsilon_s/\varepsilon_0 = 11.9$ and $\varepsilon_{ox}/\varepsilon_0 = 3.9$) is scaled by reducing all dimensions by a factor of 2 and by increasing the doping density of the substrate by a factor of 4.

    Calculate the ratio of the following parameters of the scaled device relative to that of the original device. Assume constant voltage scaling without velocity saturation.

    a) The capacitance per unit area
    b) The transit time

15. Calculate the substrate doping densities for a silicon CMOS process with an aluminum gate ($\Phi_M = 4.1$ V), an nMOS threshold voltage of 1.5 V and a pMOS threshold of –1.5 V. The oxide thickness equals 50 nm. (Assume there is no charge in the oxide and $T = 300$ K). ($\chi = 4.05$ V, $\varepsilon_{ox}/\varepsilon_0 = 3.9$, $\varepsilon_s/\varepsilon_0 = 11.9$, $n_i = 10^{10}$ cm^{-3})

16. The gate length of a silicon nMOSFET is reduced from 0.18 μm to 0.13 μm. At the same time the doping density of the substrate is increased from 8 x 10^{17} cm^{-3} to 1.2 x 10^{18} cm^{-3} and the gate oxide thickness is reduced from 6 to 4 nm.

    a) By what amount must the charge density (per unit area) at the interface be changed to reduce the threshold voltage from 0.15 V to 0.1 V? Indicate whether the charge density must be increased or decreased. The gate material is heavily doped n-type poly-silicon with a work function of 4 V.
    b) Find the threshold voltage of the 0.13 μm device if the bulk-to-source voltage equals –4 V.

17. An n-type MOSFET ($L = 1$ μm, $t_{ox} = 15$ nm, $V_T = 1$ V and $\mu_n = 300$ cm^2/V-sec, $\varepsilon_{ox}/\varepsilon_0 = 3.9$) must provide a current of 20 mA at a drain-source voltage of 2 Volt and a gate-source voltage of 5 Volt.

    a) How wide should the gate be?
    b) What is the transconductance for $V_{DS} = 4$ V and $V_{GS} = 5$ V?

18. An n-type MOSFET with a 1 micron long and 1 micron wide gate is biased at a gate source voltage which is 5 Volts larger that threshold voltage.

    a) Calculate the resistance between the source and the drain at small source-drain voltages
    b) What is the drain current if the drain-source voltage equals 1 Volt?